Claims

1. A method of fabricating a diode on a substrate, said method comprising:

forming a semiconductor layer on said substrate;

forming a first region of a first carrier concentration in said semiconductor layer;

forming a second region of a second carrier concentration in said semiconductor layer;

forming an insulator layer on said semiconductor layer;

etching said insulator layer to form at least a contact window; and

forming a metal layer on said insulator layer;

wherein said contact window exposes a portion of an upper surface of said semiconductor layer, said metal layer fills up said contact window to contact said semiconductor layer.

2. The method of claim 1, wherein said diode is formed by a thin-film transistor process, and said diode is applied to a circuit.

3. The method of claim 2, wherein said first region is adjacent to said second region.

4. The method of claim 2, further comprising forming a third region in said semiconductor layer before said step of forming said insulator layer, wherein said third region is intrinsic, said first region separates from said second region, said third region locates between said first region and said second region.

5. The method of claim 2, further comprising forming a third region of a third carrier concentration in said semiconductor layer before said step of forming said insulator layer, wherein said third carrier concentration is of a first conductivity type, said third carrier concentration is smaller than said first carrier concentration, said first region separates from said second region, said third region locates between said first region

and said second region, said third region is adjacent to said first region.

6. The method of claim 5, further comprising forming a fourth region in said semiconductor layer before said step of forming said insulator layer, wherein said fourth region is intrinsic, said third region separates from said second region, said fourth region locates between said third region and said second region.

7. The method of claim 5, further comprising forming a fourth region of a fourth carrier concentration in said semiconductor layer before said step of forming said insulator layer, wherein said fourth carrier concentration is of a second conductivity type, said fourth carrier concentration is smaller than said second carrier concentration, said third region separates from said second region, said fourth region locates between said third region and said second region, said fourth region is adjacent to said second region.

8. The method of claim 7, further comprising forming a fifth region in said semiconductor layer before said step of forming said insulator layer, wherein said fifth region is intrinsic, said third region separates from said fourth region, said fifth region locates between said third region and said fourth region.

9. The method of claim 7, further comprising forming a fifth region of a fifth carrier concentration in said semiconductor layer before said step of forming said insulator layer, wherein said fifth carrier concentration is of said first conductivity type, said fifth carrier concentration is smaller than said third carrier concentration, said third region separates from said fourth region, said fifth region locates between said third region and said fourth region.

10. The method of claim 9, wherein said second conductivity type is a negative type if said first conductivity type is a positive type, said second conductivity type is a positive type if said first conductivity type is a negative type.

11. A diode, comprising:

a semiconductor layer, comprising:

a first region of a first carrier concentration, wherein said first carrier concentration is of a first conductivity type;

a second region of a second carrier concentration, wherein said second carrier concentration is of a second conductivity type;

an insulator layer disposed on said semiconductor layer, said insulator layer including at least a contact window; and

a metal layer disposed on said insulator layer;

wherein said contact window exposes a portion of an upper surface of said semiconductor layer, said metal layer fills up said contact window to contact said semiconductor layer.

12. The diode of claim 11, wherein said diode is formed by a thin-film transistor process, said diode is applied to a circuit.

13. The diode of claim 12, wherein said first region is adjacent to said second region.

14. The diode of claim 12, wherein said semiconductor layer further comprises a third region, said third region is intrinsic, said first region separates from said second region, said third region locates between said first region and said second region.

15. The diode of claim 12, wherein said semiconductor layer further comprises a third region of a third carrier concentration, said third carrier concentration is of said first conductivity type, said third carrier concentration is smaller than said first carrier concentration, said first region separates from said second region, said third region locates between said first region and said second region, said third region is adjacent to said first region.

16. The diode of claim 15, wherein said semiconductor layer further comprises a fourth

region, said fourth region is intrinsic, said third region separates from said second region, said fourth region locates between said third region and said second region.

17. The diode of claim 15, wherein said semiconductor layer further comprises a fourth region of a fourth carrier concentration, said fourth carrier concentration is of said second conductivity type, said fourth carrier concentration is smaller than said second carrier concentration, said third region separates from said second region, said fourth region locates between said third region and said second region, said fourth region is adjacent to said second region.

18. The diode of claim 16, wherein said semiconductor layer further comprises a fifth region, said fifth region is intrinsic, said third region separates from said fourth region, said fifth region locates between said third region and said fourth region.

19. The diode of claim 16, wherein said semiconductor layer further comprises a fifth region of a fifth carrier concentration, said fifth carrier concentration is of said first conductivity type, said fifth carrier concentration is smaller than said third carrier concentration, said third region separates from said fourth region, said fifth region locates between said third region and said fourth region.

20. The diode of claim 19, wherein said second conductivity type is a negative type if said first conductivity type is a positive type, said second conductivity type is a positive type if said first conductivity type is a negative type.